CLAIMS

While the invention has been described in connection with a preferred embodiment, it is not intended to limit the scope of the invention to the particular form set forth, but on the contrary, it is intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A digital baseband receiver of low complexity for demodulation and detection in EDGE wireless cellular systems comprising:

an accurate estimator for wireless channel response;

a prefiler and DFE filter design and implementation;

a time-reversed block processor;

a forward block processor;

a soft-output equalizer integrating forward and reversed DFE outputs through convex combination;

an option of utilizing maximum a-posteriori (MAP) bi-directional equalizer in lieu of the bi-directional DFE consisting of forward and reverse soft-output Viterbi processing blocks;

a MAP outer decoder after de-interleaver to generate soft bit output information, the soft bit output information being feed back to interleaver before used by

the equalizer as extrinsic information, the exchange of soft information between equalizer and decoder forming an iterative process to be terminated by a control block monitoring the quality of extrinsic output of the MAP decoder.

2. The digital baseband receiver of claim 1 wherein

a) the channel estimator for wireless channel response defines an accurate estimator to obtain unknown channel responses through transmitted training data, said estimator being able to determine a forward finite impulse response (FIR) forward filter and an FIR decision feedback filter to be used in soft-output equalizer.

b) the prefilter defines a FIR filter with coefficients derived from results of the accurate estimator defined in claim 2.

c) the time-reversed block processor defines a time-reversal device that utilizes memory to store received data in a time-reversed order for reverse block processing.

d) The digital baseband receiver of claim1 wherein the low complexity equalizer takes convex combination of the forward DFE output and the time-reversed DFE output to define a soft input and soft output bit information to be forwarded to the interleaver and the MAP decoder.

e) The digital baseband receiver of claim1 wherein the soft-output Viterbi signal detector defines a soft-input, soft-output viterbi detector, a hard-decision unit to obtain binary information, a decision unit to determine if further iterative operation is required.

f) The digital baseband receiver of claim1 wherein the detection controller defines a control unit to control iterative process based on a criterion to

warrant a given performance requirement.

3. The baseband receiver system in claim 1 wherein said MAP decoding algorithm means includes means for generating iterative sequences of soft output values for each coded bits and message bits representing log likelihood ratio.

4. The baseband receiver system in claim 1 wherein said bi-directional equalizer includes means based on forward and time-reversed block processing and combining to generate soft symbol and bit information for outer decoder applications.

5. The baseband receiver system in claim 1 wherein said input signal includes signals obtained from down-converting and sampling single and multiple antenna RF outputs.

6. The baseband receiver system in claim 1 wherein said sampler includes baud rate and higher rate samples to generate equalizer input signals.

ABSTRACT OF DISCLOSURE

A process for signal detection in EDGE cellular systems is presented with the step of wireless channel estimation, a time-reversed signal processor, a soft-output Viterbi signal detector consisting of forward and reverse block processing, a MAP decoder that exchange soft information with the equalizer. Claim 1. A signal detection mechanism to demodulate received data frame that includes an accurate estimator to obtain channel responses, a forward filter and a FIR decision feedback filter to be used

in soft-output equalizer, a time-reversal device storing received data in a time-reversed order for reverse block processing, an interference removal apparatus in both forward and reverse processing blocks,

and a soft-input soft-output reduced state equalizer that utilizes the forward processing and reversed time processing blocks to generate iterative soft-output signals to the forward error correction decoder within the receiver system.